REMARKS

The present Amendment is in response to the Examiner's Office Action mailed August

24, 2004. Claims 6, 12, and 15 are amended. Claims 1-24 are now pending in view of the above

amendments.

Reconsideration of the application is respectfully requested in view of the above

amendments to the claims and the following remarks. For the Examiner's convenience and

reference, Applicant's remarks are presented in the order in which the corresponding issues were

raised in the Office Action.

Please note that the following remarks are not intended to be an exhaustive enumeration

of the distinctions between any cited references and the claimed invention. Rather, the

distinctions identified and discussed below are presented solely by way of example to illustrate

some of the differences between the claimed invention and the cited references. In addition,

Applicants request that the Examiner carefully review any references discussed below to ensure

that Applicants understanding and discussion of the references, if any, is consistent with the

Examiner's understanding.

I. OBJECTION TO THE SPECIFICATION

The specification is objected to because at Page 7 Line 19 the base should be referenced

as "18" instead of "16". The specification has been amended to properly reference the base as

"18" as suggested by the Examiner. Withdrawal of the objection to the specification is

respectfully requested.

II. PRIOR ART REJECTIONS

Rejections Under 35 U.S.C. §102(b)

The Examiner rejects claims 1-24 under 35 U.S.C. § 102(b) as being anticipated by U.S.

Pat. No 5,414,370 to Hashinaga et al. Because Hashinaga does not teach or suggest each and

every element of the rejected claims as currently presented, Applicants respectfully traverse the

rejection in view of the following remarks.

9

Hashinaga teaches a burn-in apparatus and method that can selectively control junction temperatures of respective semiconductor chips of a plurality of semiconductor devices during burn-in testing. (Col. 2, lines 25-29). The Hashinaga invention comprises a plurality of semiconductor devices incorporating semiconductor chips mounted to a burn-in board. (Col. 2, lines 30-39). Temperature sensors are built into the respective semiconductor chips, and are configured to measure the junction temperatures of the respective semiconductor chips. (Col. 2, lines 30-39). Figures 1-3 of Hashinaga depict a burn-in apparatus and method including a plurality of burn-in boards and semiconductor devices 33 mounted on each burn in board by sockets. (Col. 4, lines 12-16). Each semiconductor device 33 has a semiconductor chip 34 incorporated therein. (Col. 4, lines 16-17). An integrated circuit 36 and temperature detection diode 38, which is used as a temperature sensor 38, are formed directly on the semiconductor chip 34. (Col. 4, lines 17-21). Electric characteristics (e.g. changes of a threshold voltage) of the temperature detection diodes 38 are individually monitored to measure junction temperature of the semiconductor chips. A temperature adjusting unit 40 controls a laser beam irradiating means 50 or other heating means to control the temperature of the semiconductor devices 33 based on the signal received from the temperature detection diode located within each semiconductor device. (Col. 4, lines 21-49)

Independent claim 1 sets forth the following:

- 1. A system for testing optoelectronic devices, the system comprising:
- a burn-in rack mountable within a support structure, said burn-in rack supports a plurality of optoelectronic devices during burn-in testing and life testing, said burn-in rack with said plurality of optoelectronic devices being disposable in either a burn-in oven or within said support structure for life testing; and
- a detector assembly mounted to said support structure, said detector assembly comprising a plurality of detectors, each of said plurality of detectors aligning with one of said plurality of optoelectronic devices to detect an output of each of said plurality of optoelectronic devices during the testing.

(Emphasis added).

"To anticipate a claim, a prior art reference must disclose every limitation of the claimed invention, either explicitly or inherently." *In re Schreiber*, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997) (emphasis added); *see also* MPEP §2131. "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989) (emphasis added).

On page 2, the outstanding office action characterizes *Hashinaga* in part as follows: "a detector assembly (38) mounted to said support structure, said detector assembly comprising a plurality of detectors (38), each of said plurality of detectors (38) aligning with one of said plurality of optoelectronic devices (33) to detect an output of each of said plurality of optoelectronic devices (33) during testing."

However, referring to Figure 3 of *Hashinaga* and the associated disclosure, reference (38) is shown and described as a temperature detection diode formed on a semiconductor chip (34) and incorporated within each semiconductor device (33). (Col. 4, lines 16-21). Thus, the Applicant respectfully traverses the outstanding rejection and characterization of *Hashinaga* at least for the reason that a temperature sensor (38) cannot be reasonably interpreted to convey both a detector assembly and a plurality of detectors simultaneously, each plurality of detectors aligning with one of said plurality of optoelectronic devices to detect an output of each of said plurality of optoelectronic devices during testing when each temperature sensor (38) of *Hashinaga* is incorporated within each semiconductor device.

Since *Hashinaga* does not teach every element of the apparatus being claimed in claim 1, and therefore fails to anticipate or obviate claim 1, Applicants respectfully request that the rejection under 35 U.S.C. § 102(b) be withdrawn. Since claims 2-5 depend from claim 1, and thus inherit all the limitations of claim 1, Applicants submit that *Hashinaga* fails to anticipate or obviate claims 2-5 for at least the same reasons as Claim 1.

Claim 6 was amended to correct a formality by clarifying the output measured from the optical detectors. Independent claim 6 as currently presented sets forth the following:

6. A system for life testing laser diodes, comprising:

- a burn-in rack having a plurality of laser diode holders and electrical signal connectors for electrically coupling laser diodes mounted in said holders to a first electrical connector;
- a test apparatus configured to hold said burn-in rack and having optical detectors arranged to receive light from said laser diodes mounted to said burn-in rack and couple output signals from said optical detectors to a second electrical connector;
- a computer coupled to said first and second electrical connectors, said computer creating a drive current supplied to each laser diode and measuring the output signals received from said optical detectors.

On page 4, the outstanding office action characterizes *Hashinaga* in part as follows: "Hashinaga et al discloses (figs 1-3) a system and a method for testing optoelectronic devices, the system and method comprising: ... a test apparatus (12) configured to hold said burn-in rack (10) and having optical detectors (38) arranged to receive light from said laser diodes (33) mounted to said burn in rack (10) and couple output signals from said optical detectors (38) to a second electrical connector (the terminal connect to detecting unit 44),"

However, the Applicants respectfully traverse the characterization of *Hashinaga* in the outstanding office action. Referring to Figures 1-3 and the associated disclosure of *Hashinaga*, reference (38) is described as a "temperature detection diode" and a "temperature sensor". (Col. 4, lines 17-21). Diode theremometry is based on the temperature dependence of the forward voltage drop in a p-n junction biased at a constant current. It is well known in the art to use a diode as a temperature sensitive device, the turn-on voltage of the diode being <u>indicative of the ambient diode junction temperature</u>. *Hashinaga* describes in detail how electrical characteristics describing the junction temperature of the temperature detection diode are measured. (Col. 4, lines 38-49). *Hashinaga* does not, however disclose a test apparatus configured to hold a burn-in rack having optical detectors <u>arranged to receive light from said laser diodes</u> mounted to said burn-in rack and couple output signals from said optical detectors to a second electrical connector as specified by claim 6 of the present invention. The identical invention must be shown by *Hashinaga* in as complete detail as is contained in claim 6 and to assert such goes beyond the scope of that disclosed in *Hashinaga*.

Since *Hashinaga* does not teach every element of the apparatus being claimed in claim 6, and therefore fails to anticipate or obviate claim 6, Applicants respectfully request that the rejection under 35 U.S.C. § 102(b) be withdrawn. Since claims 7-11 depend from claim 6, and thus inherit all the limitations of claim 6, Applicants submit that *Hashinaga* fails to anticipate or obviate claims 7-11 for at least the same reasons.

Independent claim 12 as currently presented sets forth the following:

12. A system for testing optoelectronic devices, the system comprising: means for supporting a plurality of optoelectronic devices that are capable of undergoing a burn-in process;

means for detecting one or more optical signal output characteristics of said plurality of optoelectronic devices; and

means, electrically coupled to said means for supporting and said means for detecting, for delivering a drive current to each of said plurality of optoelectronic devices and for measuring an output from said means for detecting.

Claim 12 in part requires "means for detecting one or more optical signal output characteristics of said plurality of optoelectronic devices..." thereby invoking 35 U.S.C. 112 6th paragraph for purposes of analysis of this portion of the claim. See MPEP §2181. The first step in construing such a limitation is a determination of the function of the means plus function limitation. See Medtronic, Inc., v. Advanced Cardiovascular Systems, Inc. 248 F.3d 1303 (Fed. Cir. 2001)(citations omitted). The function of the limitation comes directly from the claim and 35 U.S.C. 112 6th paragraph "does not permit limitation of a means plus function claim by adopting a function different from that explicitly recited in the claim." Micro Chem., Inc. v. Great Plains Chem. Co., Inc., 194 F.3d 1250, 1257 (Fed. Cir. 1999) (emphasis added).

Claim 12 explicitly recites the function for the required means as "for detecting one or more optical signal output characteristics of said plurality of optoelectronic devices". With reference to Figures 1-3 and the associated disclosure, the detectors (38) of *Hashinaga* perform a function of measuring temperature, and not for receiving light from laser diodes as asserted in the outstanding office action on page 4. Moreover, the temperature detected can not be considered a signal output, but rather an environmental condition of the semiconductor device

33. Thus, *Hashinaga* cannot anticipate claim 12 since *Hashinaga* does not teach every element of the apparatus being claimed in claim 12, and Applicants respectfully request that the rejection under 35 U.S.C. § 102(b) be withdrawn. Since claims 13-19 depend from claim 12, and thus inherit all the limitations of claim 12, Applicants submit that *Hashinaga* fails to anticipate or obviate claims 13-19 for at least the same reasons.

Independent claim 20 sets forth the following:

- 20. A method of testing laser diodes, comprising:
- a step for mounting a burn-in rack having a plurality of optoelectronic devices to a test apparatus having an array of optical detectors;
- a step for providing a drive current to each of said plurality of optoelectronic devices;
- a step for measuring the optical power output of each optoelectronic device using said optical detectors; and
- a step for storing optical characterization data for each of said plurality of optoelectronic devices.

Claim 20 in part specifies "a step for measuring the optical power output of each optoelectronic device using said optical detectors" thereby invoking 35 U.S.C. 112 6th paragraph for purposes of analysis of this portion of the claim. See MPEP §2181. Claim 20 explicitly recites the function for the required step as "for measuring the optical power output of each optoelectronic device using said optical detectors". As described above with reference to Figures 1-3 and the associated disclosure, the detectors (38) of Hashinaga perform a step of measuring temperature, and not a step for receiving light from laser diodes as asserted in the outstanding office action on page 4. Thus, at least for these reasons Hashinaga cannot anticipate claim 20 since Hashinaga does not teach every element of the method being claimed in claim 20. Therefore, Applicants respectfully request that the rejection under 35 U.S.C. § 102(b) be withdrawn. Since claims 21-24 depend from claim 20, and thus inherit all the limitations of claim 20, Applicants submit that Hashinaga fails to anticipate or obviate claims 21-24 for at least the same reasons.

Claims 6 and 15 were amended to clarify the claimed subject matter by correcting minor informalities in the claims.

CONCLUSION

In view of the foregoing, Applicants believe the claims as amended are in allowable form. In the event that the Examiner finds remaining impediment to a prompt allowance of this application that may be clarified through a telephone interview, or which may be overcome by an Examiner's Amendment, the Examiner is requested to contact the undersigned attorney.

Dated this 24th day of January, 2005

Respectfully submitted,

E-CAlaness

ERIC L. MASCHOFF

Registration No. 36,596

Attorney for Applicant

Customer No. 022913

Telephone: (801) 533-9800

TAT0000000526V001.doc